26th International Symposium on VLSI Design and Test (VDAT-2022)

Theme: Chips to Startup for Sustainable Development

Indian Institute of Technology Jammu, India

Date: 17th – 19th July 2022

Program Schedule

Time	Day 1: July 17, 2022 (Sunday)	
07:45-09:30	**Registration (OAT, IIT Jammu)**	
	Hall - 1	**Hall - 2**
09:30-11:00	**Tutorial-1** Prof. Virendra Singh IIT Bombay **Title:** TBD	**Tutorial-2** Dr. Saravana Kumar M IIT Roorkee **Title:** Design of Continuous Time Analog to Digital Converters for wireless applications
11:00-11:30	**Tea Break**	
11:30-13:00	**Tutorial-3** Mr. Preet Yadav NXP Semiconductors **Title:** The New Era of Mobility	**Tutorial-4** Mr. Yagya Dutt Mishra Cadence Design Systems **Title:** Analog Reliability Analysis for Mission-Critical Applications
13:00-14:00	**Lunch Break**	
14:00-15:30	**Tutorial -5** Dr. Shailesh Singh Chouhan Lulea Science Park Sweden **Title:** Mixed-Signal Circuits in Deep Networks	**Tutorial-6** Mr. Kishan Mayani, Mr. Krushnakant Kori, Mr. Saumya Shah eInfochips Pvt. Ltd. **Title:** Reduce test escape by adapting advanced fault models
15:30-16:00	**Tea Break**	
16:00-17:30	**Tutorial-7** Dr. Vishal Sharma Intel Technologies India Pvt. Ltd. **Title:** Compute-in Memory: An opportunity and its design challenges for AI Edge Devices	**Tutorial-8** Mr. Shivam Soni, Mr. Nairuti Shah, Mr. Saurin Shah eInfochips Pvt. Ltd. **Title:** Testability Analysis and DFT Readiness at RTL stage

Time	Day 2: July 18, 2022 (Monday)	
07:30-08:30	**Registration (OAT, IIT Jammu)**	
08:30-09:00	Inauguration Address by Prof. Manoj S. Gaur Director, IIT Jammu and General Chair VDAT-2022	
	Dr. Satya Gupta, President VLSI Society of India	
	Address by Prof. Sudeb Das Gupta, Technical Program Chair, VDAT-2022	
	Address by Chief Guest Prof Adit Singh	
	Address by Dr. Ambika Prasad Shah, Conference Chair, VDAT-2022	
09:00-9:45	**Inaugural Talk (Hall-1)** **Speaker:** Mrs. Sunita Verma, Group Coordinator (R&D) Ministry of Electronics and Information Technology, Govt. of India **Session Chair:** Dr. Satya Gupta, VSI	
9:45-10:30	**Keynote Talk – I (Hall-1)** **Title:** The New Challenge in Testing SOCs: Detecting Timing Failures in Low Voltage Operating Modes **Speaker:** Prof Adit Singh; Godbold Endowed Chair Professor; Auburn University, USA **Session Chair:** Prof Virendra Singh, IIT Bombay	
10:30 – 10:45	**Tea Break**	
10:45 – 11:30	**Women in Engineering (WiE);** Sunita Verma, MeitY; Usha Mehta, Nirma University; Jayanthi Kasarla, Synopsys, and Other Experts **Moderator:** Dhanapathy Krishnamoorthy, Intel	
11:30 – 12:30	**Paper Presentation Session I (Devices -I) (3R+1S)** **Session Chair: Dr Jai Gopal Pandey; CEERI, Pilani** I-R1(3621): Rahul Kumar Gupta and Sanjeev Manhas. Design, Simulation and Optimization of Aluminium Nitride based Accelerometer I-R2 (5685): Chanchal Chanchal, Ajay Kumar Visvkarma and D. S. Rawal. Investigation of Traps in AlGaN/GaN HEMT Epitaxial Structure Using Conductance Method I-R3 (1334): Ajay Kumar and Rohit Dhiman. Differential Multi-bit Through Glass Vias for Three-Dimensional Integrated Circuits I-S4(759): Vivek Kumar, Jyoti Patel, Arnab Datta and Sudeb Dasgupta. FEM Modeling of Thermal Aspect of Dielectric Inserted Under Source & Drain of 5 nm Nanosheet	**Paper Presentation Session II (Analog/Mixed Signal -I) (3R+1S)** **Session Chair: Prof Saravana Kumar, IIT Roorkee** II-R1 (5387): Anmol Verma, Shubhang Srivastava and Ambika Prasad Shah. Aging Resilient and Energy Efficient Ring Oscillator for PUF design II-R2 (5040): Anshul Verma and Bishnu Prasad Das. Low Power Dual-Band Current Reuse-based LC-Voltage Controlled Oscillator with Shared Inductor for IOT Applications II-R3 (8410): Aranya Gupta, Sanjeev Kumar Manhas and Bishnu Prasad Das. Highly Non-linear Feed-Forward Arbiter PUF against Machine Learning Attacks II-S4 (6207): Divya Singh and Sajal K. Paul. Novel configuration of multi-mode universal shadow filter employing a new active block

12:30-12:45	**Session Break**	
12:45-14:00	**Paper Presentation Session III (Devices -II) (3R +1 S)** **Session Chair: Prof S. P. Tiwari, IIT, Jodhpur** III-R1 (9069): Shivendra Yadav, Deepak Joshi, Sanjib Kalita and Tushita Singh. Quantum Tunnelling and Thermionic Emission, Transistor simulation III-R2 (6288): Nitanshu Chauhan, Aniket Gupta, Govind Bajpai, Navjeet Bagga, Shashank Banchhor, Sudeb Dasgupta and Anand Bulusu. Unveiling the Impact of Interface Traps Induced on Negative Capacitance Nanosheet FET: A Reliability Perspective III-R3 (6306): Rajeewa Kumar Jaisawal, Sunil Rathore, P N Kondekar and Navjeet Bagga. Impact of Temperature on NDR Characteristics of a Negative Capacitance FinFET: Role of Landau Parameter (α) III-S5 (5146): Khushwant Sehra, Jeffin Shibu, Meena Mishra, Mridula Gupta, D. S. Rawal and Manoj Saxena. Implications of Field Plate HEMT towards Power Performance at Microwave X - Band	**Paper Presentation Session IV (Analog/Mixed Signal -II) (4R+1S)** **Session Chair: Prof. N. Bagga; IIITDM, Jabalpur** IV-R1 (5687): Neha Bajpai and Yogesh Singh Chauhan. A GaN Only Reverse Recovery Time Limiter Circuit Integrated with A Low Noise Amplifier IV-R2 (575): Ashutosh Pathy and Zia Abbas. 36nW, 16ppm/˚C, Process Invariant Sub-Bandgap Voltage Reference without Amplifier IV-R3 (4439): Mohd Asim Saeed, Deep Sehgal and Surinder Singh. Four Differential Channels, Programmable Gain, Programmable Data Rate Delta Sigma ADC IV-R4 (9603): Kavitha S, Santosh Kumar Vishvakarma and Bhupendra Singh Reniwal. An Approach towards Analog In-Memory Computing for Energy-Efficient Adder in SRAM Array IV-S5 (1532): Puneet Singh, Saroj Mondal and Krishnan Rengarajan. Low Power, Wideband SiGe HBT LNA Covering 57-64 GHz Band
14:00-15:00	**Lunch Break**	
15:00-15:45	**Keynote Talk – II** **Title:** Compact Modeling of FinFET and Nanosheet Transistors for 5nm Node and beyond **Speaker:** Prof. Yogesh Singh Chauhan; IIT Kanpur, India **Session Chair:** Prof J. N. Tudu, IIT Tirupati	
16:00-17:00	**Paper Presentation Session V Devices -II (3R)** **Session Chair: Prof D. Joshi SVNIT, Surat** V-R1 (4837): Mahesh Vaidya, Alok Naugarhiya, Shirsh Verma and Guru Prasad Mishra. Low Loss Enabled Semi-Superjunction 4H-SiC IGBT for High Voltage and Current Application V-R2 (9543): Arvind Bisht, Yogendra Pratap Pundir and Pankaj Kumar Pal. Electro-Thermal Analysis of Vertically	**Paper Presentation Session VI (Digital -I) (3R+1 S)** **Session Chair: Dr. Shailesh S. Chauhan, LTU Sweden** VI-R1 (4792): Prateek Sinha, Aniket Sharma, Nilay Naharas, Syed Farah Naz and Ambika Prasad Shah. QCA Technology based 8-bit TRNG Design for Cryptography Applications VI-R2 (1095): Jitesh Choudhary, Vishesh Bindal and Soumya J. MANA: Multi-Application Mapping onto Mesh Network-on-Chip using ANN

	Stacked Gate All Around Nano-sheet Transistor V-S1(8132) : Neelkamal Jhajharia, Sonal Yadav and Hemangee Kapoor. i-MAX: Just-In-Time Wakeup of Maximally Gated Router for Power Efficient Multiple NoC V-S5 (2584): Kingsuk Bag, Kavindra Kandpal, Kislay Deep, Sharad Verma, Manish Goswami and Shashi Prabha Yadav. Design Of A Low-Voltage Charge-Sensitive Preamplifier Interfaced With Piezoelectric Tactile Sensor For Tumor Detection	VI-R3 (1183): Priyank Kumar Prajapati and Anand Darji. Hardware design of two stage reference free adaptive filter for ECG denoising VI-S4 (7306): Anishetti Venkatesh, Chandan Kumar Jha, Vinod G U, Masahiro Fujita and Virendra Singh. Scalable Construction of Formal Error Guaranteed LUT-based Approximate Multipliers with Analytical Worst Case Error Bound
15:45-16:00	**Tea Break**	
17:00-17:30	**Open House on Curriculum for B.Tech in VLSI** **Moderator:** Satya Gupta, CEO, EPIC Foundation and President, VLSI Society of India	
17:30-18:30	**Design Contest/SRF-I** **(4 DC + 4 SRF)** **Session Chair:** Prof Mahesh Kumawat, Bennett University	**SRF-II** **(8 SRF)** **Session Chair:** Prof. Vaibhav Neema, IET-DAVV, Indore
18:30-19-30	**Travel to Banquet Hall from IIT Jammu**	
19:30-22:00	**Banquet Talk** **Speaker:** Chitra Hariharan, Engineering Strategy Head, HPG, Intel Corporation) **Banquet Dinner Venue:** Hotel Zone by the Park Jammu	

Time	Day 3: July 19, 2022 (Tuesday)	
09:00-9:45	**Keynote Talk – III** **Title:** Side Channel Attacks on Block Ciphers and Countermeasures **Speaker:** Prof Sri Parameswaran; University of New South Wales, Australia **Session Chair:** Prof Anand Darji, SVNIT, Surat	
9:45 – 11:15	**Paper Presentation Session VII (Sensors -I) (4R+1 S)** **Session Chair: Prof A. Beohar, VIT Bhopal** VII-R1 (1160): Sukanya Ghosh and Lintu Rajan. Enhanced Performance Enabled Room Temperature Hydrogen Sensor Based on Pd-Ti/ZnO Schottky TFT VII-R2 (6636): Medha Joshi, Upendra Kumar Verma and Brijesh Kumar. Role of solvents on the performance of bulk heterojunction (BHJ) organic solar cells VII-R3 (5128): Anuj Srivastava, Nishant Kumar, Nihar Ranjan Mohapatra and Hari Shankar Gupta. High Resolution Temperature Sensor Signal Processing ASIC for Cryo-Cooler Electronics VII-R4 (4547): Rahul Sharma and Harshal Nemade. Fabrication, Optimization and Testing of Photoconductively Tuned SAW Device using CBD Method	**Paper Presentation Session VIII (System Design-I) (1R+4 S)** **Session Chair: Prof B. P. Das IIT Roorkee** VIII-R1 (2451): Ramesh Kumar, Dr. Chiragkumar Patel, Ajay Kumar Singh, Vinay Kumar S, Himanshu N Patel and B Saravana Kumar. Development of Distributed Controller for Electronic Beam Steering using Indigenous Rad-Hard ASIC VIII-S2 (9745): Gaurav Kumar, Anuj Anuj, Satyadev Ahlawat and Yamuna Prasad. Low Cost Implementation of Deep Neural Network On Hardware VIII-S3 (4995): Chiragkumar B. Patel, Ganesh N. Mulay, Pooja Dhankher and Himanshu N. Patel. Tile Serial Protocol (TSP) ASIC for Distributed Controllers of Space-borne Radar VIII-S4 (6560): Jinay Dagli, Neel Shah, Mallikarjun Pidagannavar, Kailash Prasad and Joycee Mekie. Impact of Operand Ordering in Approximate Multiplication in Neural Network and Image Processing Applications VIII-S5 (7273): Aravindhan Alagarsamy, Sundarakannan Mahilmaran and Lakshminarayanan Gopalakrishnan. SMA: An effective partitioning with an amicable mapping approach for Networks-On-Chip
11:15 -11:30	**Tea Break**	
11:30-13:00	**Paper Presentation Session IX (Memories-I) (4R+ 1S)** **Session Chair: Prof Kavindra Kandpal, IIIT Allahabad** IX-R1 (3290): Shubham Singhania, Neelam Sharma, Varun Venkitaraman and Chandan Kumar Jha. CAR: Community Aware Graph Reordering for Efficient Cache Utilization in Graph Analytics	**Paper Presentation Session X (Digital -II) (3R +1 S)** **Session Chair: Prof Pooran Singh, Mahindra University** X-R1 (9132): Pooja Choudhary, Lava Bhargava, Masahiro Fujita and Virendra Singh. Synthesis of LUT based Approximating Adder Circuits with Formal Error Guarantees

	IX-R2 (7124): Wasi Uddin, Ankit Bende, Avinash Singh, Tarun Malviya, Rohit Ranjan, Kumar Priyadarshi and Udayan Ganguly. Indigenous Fab-Lab Hybrid Device Integration for Phase Change Memory for In-Memory Computing IX-R3 (8054): Ashwin Lele, Srivatsava Jandhyala, Saurabh Gangurde, Virendra Singh, Sreenivas Subramoney and Udayan Ganguly. Disrupting Low-write-energy vs. Fast-read Dilemma in RRAM to Enable L1 Instruction Cache IX-R4 (7758): Pramod Kumar Bharti and Joycee Mekie. RTQCC-14T: Radiation Tolerant Quadruple Cross Coupled Robust SRAM Design for Radiation Prone Environments IX-S5 (7315): Shalu Saini, Anil Lodhi, Anurag Dwivedi, Arpit Khandelwal and Shree Prakash Tiwari. Resistive switching behavior of TiO2/(PVP:MOS2) nanocomposite bilayer hybrid RRAM	X-R2 (9024): Srikanth Panasa and Srinivasu Bodapati. High Performance Ternary Full Adder in CNFET-Memristor Technology X-R3 (7073): Mohamed Asan Basiri M and Hariveer Inumarty. Low Cost Hardware Design of ECC Scalar Multiplication X-R4 (6797): Subrata Das, Debesh Kumar Das and Soumya Pandit. Reliability Aware Global Routing of Graphene Nanoribbon Based Interconnect X-R5 (5234): Shivangi Chandrakar, Deepika Gupta and Manoj Kumar Majumder. Signal Integrity and Power Loss Analysis for different Bump Structures in Cylindrical TSV
13:00-14:00	**Lunch Break**	
14.00-14:45	**Keynote Talk – IV** **Title:** The semiconductor crystal revolution that transformed the world **Prof P. Chakrabarti:** Director, Indian Institute of Engineering Science and Technology, Shibpur, India **Session Chair:** Prof S. K. Vishvakarma, IIT Indore	
14:45-15:15	**Shri H. S. Jatana:** Silicon Chip Manufacturing in India: Issues and Challenges	
15:15-16:15	**Poster Presentation and Networking** **P**: 9382, 5462,1161,4645, 6699, 0474, 2030, 6928, 7819, 2815, 1363 **Session Chair:** Prof. Usha Mehta and Mr. Bhupendra Vishwakarma	
16:15- 16:30	**Tea Break**	
16:30-17:30	**Panel Discussion on** “Chips to Start-up for Sustainable Development: A Joint Ecosystem of Academia and Industry in India” **Moderator:** Prof. S. K. Vishvakarma, IIT Indore	
17:30-18:00	**Valedictory Function: Award and Certificate Ceremony**	

R: Regular Paper: 15 Min for presentation + 2 Min Q&A = 17 Min
S: Short Paper: 10 Min for Presentation + 2 Min Q&A = 12 Min
P: Poster: 4 Min Presentation + 1 Min Q&A = 5 Min